MEMORY ARRAY WITH HIGH TEMPERATURE WIRING

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BACKGROUND OF THE INVENTION

Field of the Invention

[0001] The present invention relates generally to computer memory, and more specifically to semiconductor memory fabrication.

Description of the Related Art

[0002] Memory can either be classified as volatile or nonvolatile. Volatile memory is memory that loses its contents when the power is turned off. In contrast, non-volatile memory does not require a continuous power supply to retain information. Most non-volatile memories use solid-state memory devices as memory elements.

[0003] Certain conductive metal oxides (CMOs), for example, can be used as solid-state memory devices. The CMOs can retain a resistive state after being exposed to an electronic pulse, which can be delivered through two terminals. U.S. Pat. No. 6,204,139, issued March 20, 2001 to Liu et al., incorporated herein by reference for all purposes, describes some perovskite materials that exhibit such characteristics. The perovskite materials are also described by the same researchers in "Electric-pulse-induced reversible resistance change effect in magnetoresistive films," Applied Physics Letters, Vol. 76, No. 19, 8 May 2000, and "A New Concept for Non-Volatile Memory: The Electric-Pulse Induced Resistive Change Effect in Colossal Magnetoresistive Thin Films," in materials for the 2001 Non-Volatile Memory

Technology Symposium, all of which are hereby incorporated by reference for all purposes. However, the materials described in the 6,204,139 patent are not generally applicable to RAM memory because the resistance of the material, when scaled to small dimensions, is considered to be too large to make a memory with fast access times.

[0004] In US Pat. No. 6,531,371 entitled "Electrically programmable resistance cross point memory" by Hsu et al, incorporated herein by reference for all purposes, resistive cross point memory devices are disclosed along with methods of manufacture and use. The memory device comprises an active layer of perovskite material interposed between upper electrodes and lower electrodes.

[0005] Similarly, the IBM Zurich Research Center has also published three technical papers that discuss the use of metal oxide material for memory applications: "Reproducible switching effect in thin oxide films for memory applications," Applied Physics Letters, Vol. 77, No. 1, 3 July 2000, "Current-driven insulator-conductor transition and nonvolatile memory in chromium-doped $SrTiO_3$ single crystals," Applied Physics Letters, Vol. 78, No. 23, 4 June 2001, and "Electric current distribution across a metal-insulator-metal structure during bistable switching," Journal of Applied Physics, Vol. 90, No. 6, 15 September 2001, all of which are hereby incorporated by reference for all purposes.

[0006] The discovery of the resistance-changing property of certain CMOs, however, is relatively recent and has not yet been implemented in a commercial memory product. There are continuing efforts to bring a true non-volatile RAM (nvRAM) to market.

SUMMARY OF THE INVENTION

[0007] In one aspect of the invention a cross point memory array is provided. The cross point memory includes a substrate, a memory array, a bottom refractory metal layer and a top metal layer. The bottom refractory metal layer is parallel to the deposition face of the substrate and patterned into bottom conductive array lines. The top metal layer is also parallel to the deposition face of the substrate and patterned into top conductive array lines. Each memory cell of the memory array is at least partially defined by the intersection of a bottom conductive array line and a top conductive array line.

[0008] In another aspect of the invention, each memory cell of a memory array includes a multi-resistive state element formed with a high-temperature fabrication process at a high temperature. A plurality of conductive lines is beneath the multi-resistive state element and is stable at the high temperature. Additionally, a plurality of conductive lines is above the multi-resistive state element.

[0009] In yet another aspect of the invention, a method of manufacturing a memory is provided. A semiconductor substrate is initially provided. A bottom plurality of layers that are stable at a first temperature are then formed. Afterwards, a multi-resistive state element layer at the first temperature is formed. Then, a top plurality of layers is formed such that at least one of the layers in the top plurality of layers is not stable at the first temperature.

[0010] Other aspects of the invention will become apparent from the following detailed description taken in conjunction with the accompanying drawings which illustrate, by way of example, the principles of the invention.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention may best be understood by reference to the following description taken in conjunction with the accompanying drawings, in which:

FIG. 1A depicts a perspective view of an exemplary cross point memory array employing a single layer of memory;

FIG. 1B depicts a perspective view of an exemplary stacked cross point memory array employing four layer of memory;

FIG. 2A depicts a plan view of selection of a memory cell in the cross point array depicted in FIG. 1A;

FIG. 2B depicts a perspective view of the boundaries of the selected memory cell depicted in FIG. 2A;

FIG. 3 depicts a generalized representation of a memory cell that can be used in a transistor memory array; and

FIG. 4 depicts an exemplary flow chart of various processing steps that could be involved in fabrication of a memory.

It is to be understood that, in the drawings, like reference numerals designate like structural elements. Also, it is understood that the depictions in the FIGs. are not necessarily to scale.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0011] In the following description, numerous specific details are set forth to provide a thorough understanding of the present invention. It will be apparent, however, to one skilled in the art that the present invention may be practiced without some or all of these specific details. In other instances, well known process steps have not been described in detail in order to avoid unnecessarily obscuring the present invention.

Overview

[0012] Some memory materials require high temperature process steps in order to achieve desired properties, such as crystallinity or dopant concentration. During fabrication, a memory material is deposited on structures that may include metal lines and barrier layers. Such structures are then exposed to the high temperature processing steps and should be resistant to such temperatures.

The Memory Array

[0013] Conventional nonvolatile memory requires three terminal MOSFET-based devices. The layout of such devices is not ideal, usually requiring an area of at least $8f^2$ for each memory cell, where f is the minimum feature size. However, not all memory elements require three terminals. If, for example, a memory element is capable of changing its electrical properties (e.g., resistivity) in response to a voltage pulse, only two terminals are required. With only two terminals, a cross point array layout that allows a single cell to be fabricated to a size of $4f^2$ can be utilized. Co-

pending U.S. patent application, "Cross Point Memory Array Using Multiple Thin Films," U.S. Application No. 10/330,512, filed December 26, 2002, incorporated herein by reference in its entirety and for all purposes, describes such a device.

[0014] FIG. 1A depicts a perspective view of an exemplary cross point memory array 100 employing a single layer of memory. A bottom layer of x-direction conductive array lines 105 is orthogonal to a top layer of y-direction conductive array lines 110. The x-direction conductive array lines 105 act as a first terminal and the y-direction conductive array lines 110 act as a second terminal to a plurality of memory plugs 115, which are located at the intersections of the conductive array lines 105 and 110. The conductive array lines 105 and 110 are used to both deliver a voltage pulse to the memory plugs 115 and carry current through the memory plugs 115 in order to determine their resistive states.

[0015] Depending upon the material, a conductive array line would typically cross between 64 and 8192 perpendicular conductive array lines. Fabrication techniques, feature size and resistivity of material may allow for shorter or longer lines. Although the x-direction and y-direction conductive array lines can be of equal lengths (forming a square cross point array) they can also be of unequal lengths (forming a rectangular cross point array).

[0016] FIG. 2A illustrates selection of a memory cell 205 in the cross point array 100. The point of intersection between a single x-direction conductive array line 210 and a single y-direction conductive array line 215 uniquely identifies the single memory cell 205. FIG. 2B illustrates the boundaries of the selected memory cell 205. The memory cell is a repeatable unit that can be theoretically extended in one, two or even three dimensions. One method of repeating the memory cells in the z-direction

(orthogonal to the x-y plane) is to use both the bottom and top surfaces of conductive array lines 105 and 110.

[0017] FIG. 1B depicts an exemplary stacked cross point array 150 employing four memory layers 155, 160, 165, and 170. The memory layers are sandwiched between alternating layers of x-direction conductive array lines 175, 180 and 185 and y-direction conductive array lines 190 and 195 such that each memory layer 155, 160, 165, and 170 is associated with only one x-direction conductive array line layer and one y-direction conductive array line layer. Although the top conductive array line layer 185 and bottom conductive array line layer 175 are only used to supply voltage to a single memory layer 155 and 170, the other conductive array line layers 180, 190, and 195 can be used to supply voltage to both a top and a bottom memory layer 155, 160, 165, or 170. Co-pending U.S. patent application, "Re-Writable Memory With Multiple Memory Layers," U.S. Application No. 10/612,191, filed July 1, 2003, incorporated herein by reference in its entirety for all purposes, describes stacked cross point arrays.

[0018] Referring back to FIG. 2B, the repeatable cell that makes up the cross point array 100 can be considered to be a memory plug 255, plus 1/2 of the space around the memory plug, plus 1/2 of an x-direction conductive array line 210 and 1/2 of a y-direction conductive array line 215. Of course, 1/2 of a conductive array line is merely a theoretical construct, since a conductive array line would generally be fabricated to the same width, regardless of whether one or both surfaces of the conductive array line was used. Accordingly, the very top and very bottom layers of conductive array lines (which use only one surface) would typically be fabricated to the same size as all other layers of conductive array lines.

[0019] One benefit of the cross point array is that the active circuitry that drives the cross point array 100 or 150 can be placed beneath the cross point array, therefore reducing the footprint required on a semiconductor substrate. Co-pending U.S. patent application, "Layout Of Driver Sets In A Cross Point Memory Array," U.S. Application No. 10/612,733, filed July 1, 2003, incorporated herein by reference in its entirety for all purposes, describes various circuitry that can achieve a small footprint underneath both a single layer cross point array 100 and a stacked cross point array 150. Further details of the peripheral circuitry are described in co-pending U.S. patent application, "An Adaptive Programming Technique for a Re-Writeable Conductive Memory Device," U.S. Application No. 10/680,508, filed October 6, 2003, incorporated herein by reference in its entirety for all purposes.

[0020] The cross point array is not the only type of memory array that can be used with a two-terminal memory element. For example, a two-dimensional transistor memory array can incorporate a two-terminal memory element. While the memory element in such an array would be a two-terminal device, the entire memory cell would be a three-terminal device.

[0021] FIG. 3 is a generalized diagrammatic representation of a memory cell 300 that can be used in a transistor memory array. Each memory cell 300 includes a transistor 305 and a memory plug 310. The transistor 305 is used to permit current from the data line 315 to access the memory plug 310 when an appropriate voltage is applied to the select line 320, which is also the transistor's gate. The reference line 325 might span two cells if the adjacent cells are laid out as the mirror images of each other. Co-pending U.S. patent application, "Non-Volatile Memory with a Single Transistor and Resistive Memory Element," U.S. Application No. 10/249,848, filed

May 12, 2003, incorporated herein by reference in its entirety for all purposes, describes the specific details of designing and fabricating a transistor memory array.

The Memory Plug

[0022] Each memory plug 255 or 310 contains a multi-resistive state element (described later) along with any other materials that may be desirable for fabrication or functionality. For example, the additional materials might include a non-ohmic device, as is described in co-pending application "High Density NVRAM," U.S. Application No. 10/360,005, filed February 7, 2003, incorporated herein by reference in its entirety for all purposes. The non-ohmic device exhibits a very high resistance regime for a certain range of voltages (V_{NO-} to V_{NO+}) and a very low resistance regime for voltages above and below that range. The non-ohmic device, either alone or in combination with other elements, may cause the memory plug 255 or 310 to exhibit a non-linear resistive characteristic. Exemplary non-ohmic devices include three-film metal-insulator-metal (MIM) structures and back-to-back diodes in series.

[0023] Furthermore, as described in "Rewriteable Memory With Non-Linear Memory Element," U.S. Application No. 10/604,556, filed July 30, 2003, incorporated herein by reference in its entirety for all purposes, it may also be possible for the memory cell exhibit non-linear characteristics without a separate non-ohmic device. It should be noted that since it is possible for a memory cell to exhibit non-linear characteristics the terms "resistive memory" and "resistive device" also apply to memories and devices showing non-linear characteristics, and can also be referred to as "conductive memory" and "conductive device." While a non-ohmic device might be desirable in certain arrays, it may not be helpful in other arrays.

[0024] Electrodes will typically be desirable components of the memory plugs 255 or 310, a pair of electrodes sandwiching the multi-resistive state element. If the only purpose of the electrodes is as a barrier to prevent metal inter-diffusion, then a thin layer of metal, e.g. TiN, Pt, Au, Ag and Al. could be used. However, conductive oxide electrodes may provide advantages beyond simply acting as a metal inter-diffusion barrier. Co-pending U.S. patent application, "Conductive Memory Device With Barrier Electrodes," U.S. Application No. 10/682,277, filed October 8, 2003, incorporated herein by reference in its entirety for all purposes, describes electrodes (formed either with a single layer or multiple layers) that prevent the diffusion of metals, oxygen, hydrogen and water, act as a seed layer in order to form a good lattice match with the conductive memory element, include adhesion layers, and reduce stress caused by uneven coefficients of thermal expansion, and provide other benefits. Additionally, the choice of electrode layers in combination with the multi-resistive state element layer may affect the properties of the memory plug 255 or 310, as is described in co-pending U.S. patent application, "Resistive Memory Device With A Treated Interface," U.S. Application No. 10/665,882, filed September 19, 2003, incorporated herein by reference in its entirety for all purposes. The multi-resistive state element will generally (but not necessarily) be crystalline -- either as a single crystalline structure or a polycrystalline structure. One class of multi-resistive state element are perovskites that include two or more metals, the metals being selected from the group consisting of transition metals, alkaline earth metals and rare earth metals. The perovskites can be any number of compositions, including manganites (e.g., $Pr_{0.7}Ca_{0.3}MnO_3$, $Pr_{0.5}Ca_{0.5}MnO_3$ and other PCMOs, LCMOs, etc.), titanates (e.g., STO:Cr), zirconates (e.g., SZO:Cr), other materials such as $Ca_2Nb_2O_7$:Cr, and Ta_2O_5:Cr, and high Tc superconductors (e.g., YBCO). Specifically, MnO_3, when

combined with the rare earth metals La, Pr or some combination thereof and the alkaline earth metals Ca, Sr or some combination thereof have been found to produce a particularly effective multi-resistive state element for use in the memory plug 255 or 310. The compounds that make up the perovskite class of multi-resistive state elements include both simple conductive metal oxides and complex conductive metal oxides. Further, some oxides that may not be conductive in their pure form may be used as they become conductive through the addition of dopants, or if they are used as a very thin layer (e.g., in the order of tens of Angstroms) in which case tunneling conduction can be achieved. Therefore, as will be appreciated by those skilled in the art, the terms "conductive memory" and "conductive device" can include devices that are fabricated with materials that are classified as insulators, but are thin enough to allow tunneling conduction.

[0025] Multi-resistive state elements, however, are not limited to perovskites. Specifically, any material that has a hysteresis that exhibits a resistive state change upon application of a voltage while allowing non-destructive reads is a good candidate for a multi-resistive state element. A non-destructive read means that the read operation has no effect on the resistive state of the memory element. Measuring the resistance of a memory cell is accomplished by detecting either current after the memory cell is held to a known voltage, or voltage after a known current flows through the memory cell. Therefore, a multi-resistive state material that is placed in a high resistive state R_0 upon application of $-V_W$ and a low resistive state R_1 upon application of $+V_W$ should be unaffected by a read operation performed at $-V_R$ or $+V_R$. In such materials a write operation is not necessary after a read operation. The same principle applies if more that one resistive state is used to store information (e.g., the multi-resistive state element has a high resistive state of R_{00}, a medium-high

resistive state of R_{01}, a medium-low resistive state of R_{10} and a low resistive state of R_{11}).

[0026] As described in co-pending U.S. patent application, "A 2-Terminal Trapped Charge Memory device with Voltage Switchable Multi-Level Resistance," U.S. Application No. 10/634,636, filed August 4, 2003, incorporated herein by reference in its entirety for all purposes, trapped charges are one mechanism by which the hysteresis effect is created. Trapped charges can be encouraged with dopants, as described in co-pending U.S. patent application, "Multi-Resistive State Material that Uses Dopants," U.S. Application No. 10/604,606, filed August 4, 2003, incorporated herein by reference in its entirety for all purposes.

Fabrication

[0027] FIG. 4 is an exemplary flow chart of various processing steps that could be involved in fabrication of a memory. At 405, standard front end of line (FEOL) processes can be used to form the active circuitry that drives the cross point memory array. FEOL processes are generally defined as operations performed on a semiconductor wafer in the course of device manufacturing up to first metallization, and might end with chemical-mechanical polishing (CMP) of an inter-layer dielectric (ILD). Certain cross point arrays, especially those with active circuitry underneath the memory array, might also include various metallization layers in step 405. The metallization layers are used to electrically connect the active circuitry to the conductive array lines of the cross point array 100 or 150.

[0028] The next processing step at 410 is formation of contact holes through the ILD to appropriate positions in the active circuitry (or metallization layers in the case of some cross point arrays) followed by plug formation at 415. Certain transistor

memory arrays may require these steps if, for example, the memory plug 310 were so wide that it would overlap the transistor's gate 320. Otherwise, the memory plug 310 could be formed directly on top of the semiconductor substrate 305.

[0029] Once the plugs are formed, a cross point array 100 or 150 would require that the conductive array lines be patterned on the wafer at 420. If refractory metals with relatively high resistivities are used for the conductive array lines, the maximum length and minimum cross-sectional area may be limited in comparison to aluminum or copper.

[0030] Another ILD layer could be deposited over the first layer of conductive array lines at 425. The dielectric layer can be deposited over the conductive array lines by plasma-enhanced chemical vapor deposition (PECVD) and then planarized by CMP to expose the top surfaces of the conductive array lines.

[0031] At 430 the memory plug formation begins. In the case of transistor memory array, the memory plug can be formed directly on the contact hole plugs. In the case of a cross point array, the memory plugs are formed on the bottom conductive array lines.

[0032] Regardless of the memory array, a memory plug generally begins with the deposition of the bottom electrodes at 430. At 435 the multi-resistive state elements are deposited, typically using high temperature processing (e.g., solution based spin on followed by high temperature anneal, pulsed laser deposition, sputtering, and metal-organic chemical vapor deposition). However, co-pending U.S. patent applications, "Laser Annealing of Complex Metal Oxides (CMO) Memory Materials for Non-Volatile Memory Integrated Circuits," U.S. Application No. 10/387,799, and "Low Temperature Deposition of Complex Metal Oxides (CMO) Memory Materials for Non-Volatile Memory Integrated Circuits," U.S. Application No. 10/387,799, both

filed March 13, 2003, and both incorporated herein by reference in their entireties for all purposes, describe fabrication techniques that may be able to be used in lieu of high temperature fabrication processes. If high temperature fabrication were used, then all the circuitry elements that were deposited before the multi-resistive state element would need to withstand those high temperatures. Using refractory metals is one technique that can be used to create elements that can endure high temperatures.

[0033] It should also be appreciated that fabrication of the multi-resistive state element might include additional techniques in order to ensure an effective memory device. For example, biasing the multi-resistive state element might be beneficial in order to ensure the hysteresis is presented in a certain direction. Co-pending U.S. patent application, "Multi-Layer Conductive Memory Device," U.S. Application No. 10/605,757, filed October 23, 2003, incorporated herein by reference in its entirety for all purposes describes using a multi-layered multi-resistive state element in order to encourage a hysteresis in a certain direction.

[0034] At 440 another electrode is deposited on top of the multi-resistive state element. At 450 the optional non-ohmic device is formed. If the non-ohmic device is a MIM structure, a top electrode layer may or may not be necessary at 455. In addition, this top electrode layer could include a barrier layer to prevent metal inter-diffusion.

[0035] At 460 standard photolithography and appropriate multi-step etch processes could be used to pattern the memory/non-ohmic film stack into memory cell plugs. Co-pending U.S. patent application, "Conductive Memory Stack With Non-Uniform Width," U.S. Application No. 10/605,963, filed November 10, 2003, incorporated herein by reference in its entirety for all purposes describes an improved

fabrication technique that includes etching a memory plug with a non-uniform width and using a sidewall layer around the memory plug.

[0036] At 465 depositing another ILD, which can then be planarized by CMP, fills in the spaces between the plugs. At 470 via holes are formed in the ILD. Via holes could be formed to connect the tops of the memory cell islands and are one mechanism that can be used to provide connections between metal interconnect layers. The via holes are then filled at 475.

[0037] The top layer(s) of conductive lines could then be formed at 480. For cross point array a single conductive array line would complete the memory cell 205. For a transistor memory array the data line 315 and the reference line 325 would still need to be formed. Regardless, if there are no more memory elements to form at high temperatures, the final layer(s) of conductive lines may comprise aluminum, copper or other high conductivity metal using standard metallization processes.

High Temperature Fabrication

[0038] As previously described, the fabrication techniques used for the memory plug 255 or 310 will typically dictate the requirements of the layers beneath the memory plug (e.g., in a transistor memory array the select line 320; and in a cross point array 100 or 150 the driver circuitry and conductive lines 105, 175, 180, 190 and 195). Since certain fabrication processes (e.g., solution based spin on followed by high temperature anneal, pulsed laser deposition, sputtering, and metal-organic chemical vapor deposition) might require high temperatures, refractory metals can be used for these layers so that they may withstand the temperatures.

[0039] Typical metal lines in integrated circuits are made out of aluminum or copper. However, these metals have a rather low melting point, and the structural

integrity of the formed metal lines is damaged if they are allowed to melt. Furthermore, these materials cannot even withstand exposure to temperatures below their melting point. For example, although aluminum's melting point is 660C, it generally should not be exposed to temperatures above 400C. At such temperatures the aluminum atoms start to diffuse to other areas, possibly reacting with other semiconductor elements on the substrate, disturbing the characteristics of those elements. The diffusion increases with increasing temperatures, becoming largely unworkable at 450C.

[0040] Therefore, if typical low temperature conductive lines were used (i.e., aluminum or copper), any material above the first metal line would be limited to temperatures where they were considered to be "stable" metals. However, most manufacture processes require high temperatures to grow the crystalline or poly-crystalline structure of the multi-resistive state element. In such processes, high temperature is typically between 600C and 800C.

[0041] Therefore, using conductive lines that can withstand high temperatures is sometimes required. High melting point metals are usually referred to as refractory metals, and include tungsten, molybdenum, tantalum, niobium, chromium, vanadium and rhenium, as well as the less common zirconium, technetium, ruthenium, rhodium, hafnium, osmium and iridium. Some of the latter metals may, however, not be practical for use in an integrated circuit process. Refractory metals also include any compounds and alloys that have high melting points. Additionally, in many applications it is preferable to use a material with a low resistivity in order to both improve the memory access time and allow for longer array lines.

[0042] Additionally, any conductive material with a melting point of at least 100C above the desired process temperature can typically be used. For example, in the case

of aluminum, a desired process temperature 200C below the melting point of aluminum is generally preferred. Therefore, an optimum conductive array line would be a refractory metal with a low resistivity that has a melting point at least 100C above the high temperature processing that is used.

[0043] Conductive lines are not the only elements that may need to withstand high temperature processing. Typically, only the layers that are deposited after the high temperature processing of the memory plug are free from high temperatures. Since no high temperature steps are required after the memory plug's formation, the top layers of the memory do not need to have high melting points. Therefore, such layers can be made with standard metallization materials such as aluminum, copper or aluminum alloys such as aluminum-silicon, aluminum-silicon-copper or aluminum-copper.

[0044] The elements that may need to withstand high temperature processing can include the multi-resistive state material, a possible non-ohmic device, appropriate electrodes, bottom layers of conductive array lines, and contact plugs to connect the electrodes of the memory cells to the conductive array lines. Electrodes made out of noble metals, binary or ternary oxides and nitrides, and conductive metal oxides are temperature resistant and have been described in detail in co-pending U.S. patent application, "Conductive Memory Device With Barrier Electrodes," U.S. Application No. 10/682,277, filed October 8, 2003, already incorporated by reference. The same application additionally describes sacrificial layers that can act as an oxygen barrier by reacting with oxygen while remaining electrically conductive. Examples of high temperature resistant materials that can act as a sacrificial layers include ternary oxides such as ruthenium tantalum oxide, ruthenium titanium oxide, iridium tantalum oxide or iridium titanium oxide and ternary nitrides such as ruthenium tantalum

nitride, ruthenium titanium nitride, iridium tantalum nitride or iridium titanium nitride.

Concluding Remarks

[0045] Although the invention has been described in its presently contemplated best mode, it is clear that it is susceptible to numerous modifications, modes of operation and embodiments, all within the ability and skill of those familiar with the art and without exercise of further inventive activity. Accordingly, that which is intended to be protected by Letters Patent is set forth in the claims and includes all variations and modifications that fall within the spirit and scope of the claim.